UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,539	04/14/2004	Ayako Nakano	04329.3304	4440

22852 7590 06/01/2007

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
ROSASCO, STEPHEN D	

ART UNIT	PAPER NUMBER
1756	

MAIL DATE	DELIVERY MODE
06/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,539	NAKANO ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *13-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Applicant's election without traverse of Group I (claims 1-12 and 25) in the reply filed on 4/02/07 is acknowledged.

Claim 2 is objected to because of the following informalities: last 2 lines, "and the layers includes the patterns concurrently arranged each other."

Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Kotani et al. (6,853,743) orYamauchi (2005/0034093).

The claimed invention is directed to a pattern forming method of forming a desired pattern on a semiconductor substrate comprising: extracting a first pattern of a layer; extracting a second pattern of one or more layers overlapped with the layer, the second pattern being arranged close to or overlapped with the first pattern;

calculating a distance between the first and second patterns on a semiconductor substrate in consideration of a predetermined process variation; determining whether or not the distance between the first and second patterns satisfy an allowable margin given for the distance between the first and second patterns;

and correcting, if the distance does not satisfy the allowable margin, at least one of the first and second patterns to satisfy the allowable margin.

And wherein the first and second patterns comprise one of a design pattern and a mask pattern formed on a mask, and the layers includes the patterns concurrently arranged each other.

And wherein the process variation includes at least one of a variation of an exposure quantity of an exposure apparatus, a variation of a focal distance, a variation of an exposure irradiation, a variation of a lens aberration, a variation of a mask dimension, a variation of a development process, and a variation of an etching process.

Kotani et al. (see claim 1) addresses claims 1-12 and 25 – including a mask pattern correction method comprising the step of extracting a correction target edge from a design pattern, the step of calculating the distance from the correction target edge to the nearest edge of an adjacent pattern, the step of calculating the correction value by a simulation in accordance with a pattern layout present within a given range determined by the correction target edge, and moving the correction target edge on the basis of the calculated correction value when the distance calculated in the distance calculation step is smaller than a predetermined distance, and the step of moving the correction target edge on the basis of an correction value set as a rule in advance in accordance with the distance when the distance calculated in the distance calculation step is larger than the predetermined distance.

Yamauchi (see claims 23-50) addresses claims 1-12 and 25, including a method for designing a semiconductor integrated circuit device, the method comprising the step of: forming, on a substrate, a plurality of design patterns composed of circuit elements or

wires, wherein a plurality of design rules having different values are applied to the plurality of design patterns by using dependence of respective finished sizes of the design patterns on a geometric feature of each of the design patterns.

And wherein the geometric feature is a layout density of the circuit elements or the wires on the substrate and the design rules are set to correct dependence of the finished sizes on the layout density.

And wherein the geometric feature is the presence or absence of a dummy pattern which is a dummy of each of the design patterns contained therein and if the dummy patterns are contained in the design pattern, the design rules are set to correct dependence of the finished size on the dummy pattern.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
05/25/07